CLAIMS

1. A method of forming a plurality of integrated circuit die on a semiconductor wafer, comprising:

forming a first integrated circuit die in a first area in a fixed position relative to the semiconductor wafer, comprising the steps of:

forming at least two devices in the first area, the at least two devices selected from a group of active and passive devices;

forming a first metal layer comprising portions connecting to the at least two devices in the first area;

forming a second integrated circuit die in a second area in a fixed position relative to the semiconductor wafer, the second area separated from the first area by a scribe area, comprising the steps of:

forming at least two devices in the second area, the at least two devices selected from a group of active and passive devices;

forming the first metal layer to further comprise portions connecting to the at least two devices in the second area;

forming the first metal layer to further comprise a portion electrically connecting a portion of the first metal layer in the first area to a portion of the first metal layer in the second area and thereby extending in the scribe area.

2. The method of claim 1 and further comprising the step of physically separating the first integrated circuit die from the second integrated circuit die.

3. The method of claim 2 wherein the step of separating comprises cutting the semiconductor wafer.

4. The method of claim 3 wherein the step of cutting operates to sever the portion electrically connecting a portion of the first metal layer in the first area to a portion of the first metal layer in the second area.

5. The method of claim 2 wherein the step of physically separating operates to sever the portion electrically connecting a portion of the first metal layer in the first area to a portion of the first metal layer in the second area.

6. The method of claim 1 and further comprising forming an electrical contact in electrical communication with the portion electrically connecting a portion of the first metal layer in the first area to a portion of the first metal layer in the second area.

7. The method of claim 6 and further comprising a step of simultaneously testing the first integrated circuit die and the second integrated circuit die by communicating a test signal between a test apparatus and the electrical contact.

8. The method of claim 6 wherein the step of forming an electrical contact comprises forming the electrical contact in the scribe area.

9. The method of claim 6 wherein the step of forming an electrical contact comprises forming the electrical contact in the first area.

10. The method of claim 6 wherein the electrical contact comprises a first electrical contact, and further comprising the steps of:

forming a second electrical contact in the first area and in electrical communication with a portion of the first metal layer, wherein the second electrical contact is operable to communicate with the first integrated circuit after physically separating the first integrated circuit from the semiconductor wafer; and

forming a third electrical contact in the second area and in electrical communication with a portion of the first metal layer, wherein the third electrical contact is operable to communicate with the second integrated circuit after physically separating the second integrated circuit from the semiconductor wafer.

11. The method of claim 10 wherein the first electrical contact has a larger surface area than the second electrical contact and the third electrical contact.

12. The method of claim 1:

wherein the semiconductor wafer comprises a semiconductor substrate;

wherein a distance D_{max} is defined between a plane along the semiconductor substrate and a plane of an intra-die metal connecting layer formed as part of the first integrated circuit die and the second integrated circuit die; and

wherein the first metal layer is a distance from the semiconductor substrate equal to or less than D_{max}.

13. The method of claim 1 wherein the step of forming a first metal layer further comprises forming a plurality of isolated metal layer portions in the first area and each electrically isolated from one another, and further comprising forming a plurality of electrical contacts, each in electrical communication with a different one of the plurality of isolated metal layer portions.

14. The method of claim 13 wherein each of the plurality of isolated metal layer portions extends into the scribe area.

15. The method of claim 14 wherein each of the plurality of electrical contacts is located in the scribe area.

16. The method of claim 15:

wherein the plurality of electrical contacts comprises a first plurality of electrical contacts;

and further comprising forming a second plurality of electrical contacts in the first area and for communicating electrical signals with the first integrated circuit die;

wherein each of the second plurality of electrical contacts is electrically isolated from the scribe area and the second area; and

wherein the first plurality of electrical contacts outnumber the second plurality of electrical contacts.

17. The method of claim 1:

wherein the portion electrically connecting a portion of the first metal layer in the first area to a portion of the first metal layer in the second area comprises a first portion;

wherein the step of forming the first metal layer further comprises:

forming a second portion of the first metal layer in the first area and for communicating electrical signals with respect to the first integrated circuit die; and

forming a third portion of the first metal layer in the second area and for communicating electrical signals with respect to the second integrated circuit die;

wherein the second portion is electrically disconnected from the third portion; and

further comprising forming a test circuit in the scribe area and having a first input connected to the second portion and second input connected to the third portion.

18. The method of claim 17 wherein the test circuit comprises at least one logic gate.

19. The method of claim 17 wherein the test circuit comprises a state machine.

20. The method of claim 17 wherein the test circuit comprises a multiplexer.

21. The method of claim 20 wherein the multiplexer has an output, and further comprising:

at a first time testing the first integrated circuit die by controlling the multiplexer to couple the first input to the output; and

at a second time testing the second integrated circuit die by controlling the multiplexer to couple the second input to the output.

22. The method of claim 1:

and further comprising forming a plurality of integrated circuit die on the semiconductor wafer;

wherein each of the plurality of integrated circuit die is operable to perform functionality after each of the plurality of integrated circuit die is physically separated from the semiconductor wafer; and

wherein the plurality of integrated circuit die comprises the first integrated circuit die and the second integrated circuit die;

wherein the step of forming a plurality of integrated circuit die on the semiconductor wafer comprises, for each of the plurality of integrated circuit die, the steps of:

completing circuitry for performing the functionality; and

no later than the completing step, forming a metal layer that comprises at least one intra-die portion and at least one inter-die portion.

23. The method of claim 1 wherein each of the steps of forming a first metal layer are performed using a reticle.

24. A method of forming a plurality of integrated circuit die on a semiconductor wafer, comprising:

forming each of the plurality of integrated circuit die in a respective area on the semiconductor wafer;

wherein each respective area is isolated from other respective area by a scribe area;

wherein each of the plurality of integrated circuit die is operable to perform functionality after each of the plurality of integrated circuit die is physically separated from the semiconductor wafer; and

wherein the step of forming a plurality of integrated circuit die on the semiconductor wafer comprises, for each of the plurality of integrated circuit die, the steps of:

completing circuitry for performing the functionality; and

no later than the completing step, forming a metal layer that comprises at least one intra-die portion and at least one inter-die portion, wherein the inter-die portion extends into the scribe area.

25. The method of claim 24 and further comprising forming a plurality of shared contacts in the scribe area, wherein each of the plurality of shared contacts is electrically connected to an inter-die portion of at least two of the plurality of integrated circuit die.

26. The method of claim 25 and further comprising a step of simultaneously testing a first one of the plurality of integrated circuit die and a second one of the plurality of integrated circuit die by communicating a test signal between a test apparatus and one of the plurality of shared contacts.

27. The method of claim 24 and further comprising forming a plurality of shared contacts in the scribe area, wherein each of the plurality of shared contacts is electrically connected to an inter-die portion of all of the plurality of integrated circuit die.

28. The method of claim 27 and further comprising a step of simultaneously testing all of the plurality of integrated circuit die by communicating a test signal between a test apparatus and one of the plurality of shared contacts.

29. The method of claim 24 and further comprising:

forming a plurality of shared contacts in the scribe area, wherein each of the plurality of shared contacts is electrically connected to an inter-die portion of at least two of the plurality of integrated circuit die; and

forming at least one isolated contact for each of the plurality of integrated circuit die wherein the isolated contact for each integrated circuit die is electrically isolated from all other of the plurality of integrated circuit die.

30. The method of claim 29 wherein the plurality of shared contacts outnumber a total of all of the isolated contacts.

31. A semiconductor wafer, comprising a plurality of integrated circuit die, each of the plurality of integrated circuit die in a respective area on the semiconductor wafer and isolated from all other of the plurality of integrated circuit die by a scribe area, each of the plurality of integrated circuit die comprising:

at least two devices selected from a group of active and passive devices;

a metal layer comprising at least one intra-die portion connected to the at least two devices for permitting the integrated circuit de to perform functionality after each of the plurality of integrated circuit die is physically separated from the semiconductor wafer;

at least one metal inter-die portion extending into the scribe area;

wherein the semiconductor wafer comprises a semiconductor substrate;

wherein a distance D_{max} is defined between a plane along the semiconductor substrate and a plane of the intra-die portion; and

wherein the metal inter-die portion is a distance from the semiconductor substrate equal to or less than D_{max}.

32. The semiconductor wafer of claim 31 wherein the metal layer comprises the at least one metal inter-die portion.

33. The semiconductor wafer of claim 31 and further comprising a shared contact in the scribe area, wherein the shared contact is electrically connected to the at least one metal inter-die portion of at least two of the plurality of integrated circuit die.

34. The semiconductor wafer of claim 31 and further comprising a shared contact in the scribe area, wherein the shared contact is electrically connected to the at least one metal inter-die portion of all of the plurality of integrated circuit die.

35. The semiconductor wafer of claim 31 and further comprising a plurality of shared contacts in the scribe area, wherein each of the plurality of shared contacts is electrically connected to an inter-die portion of at least two of the plurality of integrated circuit die.

36. The semiconductor wafer of claim 35 wherein each of the plurality of integrated circuit die further comprises at least one isolated contact in each of the respective areas on the semiconductor wafer, wherein the isolated contact for each integrated circuit die is electrically isolated from all other of the plurality of integrated circuit die.

37. The semiconductor wafer of claim 36 wherein the plurality of shared contacts outnumber a total of all of the isolated contacts.

38. The semiconductor wafer of claim 31 and further comprising a plurality of metal inter-die portions extending into the scribe and comprising the at least one metal inter-die portion.

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